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10/511,566	04/13/2005	Jurgen Leib	2133.063USU	4191

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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,566	LEIB ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/19/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12-17,19,20,34,39,41 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10,12-17,19,20,34,39,41 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 3-7, 9, 10, 12-17, 19, 20, 34, 39, 41 and 42 are rejected under 35 U.S.C. 103(a) as being obvious over Wada in view of Camlibel (US 4,374,391), Fleming (US 5,047,369), Baglin (US 4,001,049), and Sioshansi (US 4,855,026).

RE claim 1, Wada discloses (Figs 6-9) a process for forming a housing for electronic modules, comprising the steps of:

providing a substrate (5; ¶83 ln 1-2) having one or more regions, the one or more regions comprising at least one semiconductor structure, the substrate having at least a first substrate side (B) to be encapsulated and an underside (A), wherein the at least one semiconductor structure (13; ¶73 ln 4-6) is located on the first substrate side (B);

providing a glass source (¶113);

arranging the first substrate side in such a manner with respect to the glass source that the first substrate side can be coated (¶113);

coating the first substrate side with a glass layer (Fig 9: 9; ¶113 ln 1-2).

Wada differs from the claimed invention only in not disclosing vapor-deposition.

Camlibel teaches that glass encapsulation is particularly desirable in integrated circuits such as that of Wada (col 1 ln 33-35, col 2 ln 50, col 3 ln 8-10) and that e-beam (vapor) deposition is known in the art to be a suitable technique (col 4 ln 44-47).

Fleming teaches that glass encapsulation is particularly desirable in integrated circuits such as that of Wada (col 1 ln 63-67, col 3 ln 12-14) and that e-beam (vapor) deposition is a preferred technique, at least for reduced contamination (col 1 ln 28-32).

Baglin teaches directing an ion beam (col 2 ln 1-7) from a plasma (ionized gas is plasma: col 1 ln 57-62, col 2 ln 28-30, col 4 ln 14-29) onto a glass (SiO_2) layer of an integrated circuit such as that of Wada (col 1 ln 10-12, col 4 ln 31-33) so as to advantageously densify the glass layer (col 2 ln 31-34).

Siohansi teaches directing an ion beam from a plasma (ionized gas is plasma: col 1 ln 7-12 & 67-68, col 4 ln 11, col 5l n 1-6) onto the substrate during the vapor coating (col 1 ln 7-13, col 2 ln 3-7) to advantageously densify the deposited layer (col 2 ln 7 & 11-12; col 2 ln 60-65); which process may be used in nearly any application ("generally" and "surfaces of interest": col 1 ln 7-13; "almost any workpiece": 2 ln 55-58).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel and Fleming such that said glass source is a vapor-deposition glass source and that said coating is vapor-coating; at least for reduced contamination. See MPEP § 2144.06 and 2144.07.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Wada in view of Baglin and Sioshansi to include producing an ion beam by ionizing a gas in a plasma generated by a plasma source and directing said beam onto the substrate during the vapor coating so as to additionally densify the glass layer such that the glass layer has a helium leak rate.

Wada as modified above differs from the claimed invention only in not explicitly stating the helium leak rate.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the helium leak rate is less than the claimed value; at least to minimize leaking.

RE claim 3, Wada discloses (Fig 9) providing the substrate with a passivation layer (26; ¶136 In 5) on a second side (A) that is on the opposite side from the first substrate side (B).

RE claim 4, Wada discloses the substrate comprises a wafer (5; ¶83 In 2), the process further comprising packaging components which still form part of the wafer (¶124 In 1-5).

RE claim 5, Wada discloses coating a second substrate side with a protective film (26; ¶136 In 5).

Wada differs from the claimed invention in not disclosing vapor-coating a second substrate side with a glass layer.

Camlibel discloses (Fig 5) an analogous device (60) having the first and the opposite second sides both covered with glass layers (62, 68; col 5 In 63 – col 6 In 2), which protects the surface (col 3 In 46).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Wada in view of Camlibel to further comprising vapor-coating a second substrate side with a glass layer; at least for protection.

RE claim 6, Wada as modified above discloses the vapor-deposition glass source generates at least a binary glass system (borosilicate: Camlibel col 2 In 55).

RE claim 7, Wada as modified above discloses the first substrate side is vapor-coated until the glass layer has a thickness in the range from 0.01 to 1000 μm (Camlibel col 7 In 68; 3000 Angstroms = 0.3 μm).

RE claim 9, Wada as modified above discloses the glass layer has a thickness in the range between 0.1 and 50 μm (Camlibel col 7 In 68).

RE claim 10, Wada as modified above differs from the claimed invention only in not expressly disclosing a glass layer thickness in the range between 50 and 200 μm. Parameters such as film thickness in the art of semiconductor manufacturing are subject to routine experimentation and optimization. It would have been obvious to one of ordinary skill in the art at the time the invention was made that the glass layer have a thickness in the range between 50 and 200 μm; at least to optimize the glass layer's optical properties.

RE claim 12, Wada as modified above does not limit the borosilicate glass to any particular type, therefore the combined disclosure encompasses all well-known borosilicate glass types, including those containing aluminum oxide and alkali metal oxide fractions.

RE claim 13, Wada as modified above discloses the glass layer has a coefficient of thermal expansion that is virtually equal to that of the substrate (Camlibel: col 2 In 57-62; Fig 1, col 5 In 7-18).

RE claim 14, Wada as modified above discloses the glass layer provides a hermetic (air-tight) seal.

RE claim 15, Wada discloses coating a second substrate side with a protective film (26; ¶136 In 5).

Wada differs from the claimed invention in not disclosing vapor-coating a second substrate side with a glass layer.

Camlibel discloses (Fig 5) an analogous device (60) having the first and the opposite second sides both covered with glass layers (62, 68; col 5 In 63 – col 6 In 2), which protects the surface (col 3 In 46).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Wada in view of Camlibel to further comprising vapor-coating a second substrate side with a glass layer; at least for protection.

This combination comprises vapor depositing a plurality of glass layers onto (at least one onto the top of and at least one onto the bottom of) the substrate.

RE claim 16, Wada discloses (Fig 6F-6G) removing material from a second substrate side (¶91 In 1-2), the second substrate side being on the opposite side from the first substrate side.

RE claim 17, Wada discloses (Fig 3) the substrate includes a wafer (5) having a plurality of the structures (3; ¶83 In 1-2) wherein the process further comprises dividing the wafer to form a plurality of electronic modules which each have first encapsulated sides (¶124 In 1-5).

RE claim 19, Wada as modified above discloses vapor coating the underside with the glass layer (Fig 11: 26) after the plastic layers (Fig 7F: 66) have been removed from the underside so that the plurality of electronic modules are encapsulated on both sides.

RE claim 20, Wada as modified above differs from the claimed invention only in not expressly disclosing the glass layer on the underside has a thickness in the range from 1 to 50 μm.

Parameters such as film thickness in the art of semiconductor manufacturing are subject to routine experimentation and optimization.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that the glass layer have a thickness in the range from 1 to 50; at least to optimize the glass layer's optical properties.

RE claim 34, Wada discloses (e.g., Fig 9) applying a layer of plastic (11) below the glass layer (9; ¶75 ln 5-7).

Wada differs from the claimed invention only in not disclosing said plastic layer on a surface of the glass layer opposite the substrate.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to reverse/rearrange the order of the glass layer and plastic layer; which would not modify the device operation. See MPEP § 2144.04(VI)(A&C).

RE claim 39, Wada discloses (Figs 6) lithographing ([0085], [0089]) plastic layers (32, 42, 44) on the substrate to define the structure and removing the plastic layers from the underside (Fig 6F-6G: 44; ¶91 ln 1-2).

RE claim 41, Wada discloses the semiconductor structure comprises an integrated circuit (IC encompasses the device of Wada).

RE claim 42, Wada discloses removing loosely adhering particles from a surface (the bombardment of ions inherently removes some loosely adhering particles).

Claim 8 is rejected under 35 U.S.C. 103(a) as being obvious is view of Wada, Camlibel, Fleming, Baglin and Sioshansi as to claim 1 above, further in view of Butt.

RE claim 8, Wada as modified above does not disclose organic constituents.

Butt discloses that an organic-reinforced glass is particularly reliable and useful for hermetic sealing of electronic packages (col 2 ln 67 – col 3 ln 6, col 5 ln 11-17).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Wada in view of Butt by providing a reservoir having organic constituents and converting the organic constituents into the vapor state through the application of a vacuum so that during the vapor-coating mixed layers comprising inorganic and organic constituents can be formed on the first substrate side; at least for reliability.

If objective evidence is made of record that establishes either: that the facts in the above referenced legal decisions are not sufficiently similar to the present application; or that there is criticality to the order of parts as claimed, then the following alternate grounds of rejection of claim 34 applies.

Claim 34 is rejected under 35 U.S.C. 103(a) as being obvious in view of Wada, Camlibel, and Fleming, as applied to claim 1 above, and further in view of Xu.

RE claim 34, Wada differs from the claimed invention only in not disclosing said plastic layer above the glass layer.

Xu discloses (e.g., Fig 2) a dielectric stack of layers (16) having different indexes of refraction forming a dielectric mirror (col 3 In 35-44), i.e., designed reflection control.

Camlibel discloses using glass layers both as a dielectric mirror and to reduce reflection (col 3 In 40-56, esp. In 51-54) , i.e., designed reflection control.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel and Xu to comprise applying a layer of plastic above the glass layer; at least to reduce surface reflection. See also MPEP § 2141.03 (reflection control as applicable principle).

Response to Arguments

The arguments filed 11/19/2007 have been considered but are moot in view of the new grounds of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571- 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. For more info about PAIR, see http://pair-direct.uspto.gov. For questions PAIR access, contact the Electronic Business Center at 866-217-9197 (toll-free). For assistance from a USPTO Customer Service Rep or access to the automated info system, call 800-786-9199 or 571-272-1000.

/Carl Whitehead Jr./
Supervisory Patent Examiner, Art Unit 2813

/Andrew O. Arena/
Examiner, Art Unit 2811
3 March 2008